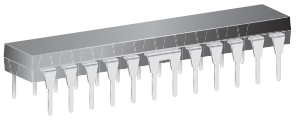
DMOS Full-Bridge PWM Motor Driver

Features and Benefits

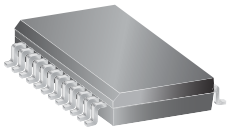
- ±3 A, 50 V Output Rating
- Low $r_{DS(on)}$ Outputs (270 mΩ, Typical)
- Mixed, Fast, and Slow Current-Decay Modes
- Synchronous Rectification for Low Power Dissipation
- Internal UVLO and Thermal-Shutdown Circuitry
- Crossover-Current Protection
- Internal Oscillator for Digital PWM Timing

Packages:

Package B, 24-pin DIP with exposed tabs



Package LB, 24-pin SOIC with internally fused pins



Package LP, 28-pin TSSOP with exposed thermal pad

Not to scale

Description

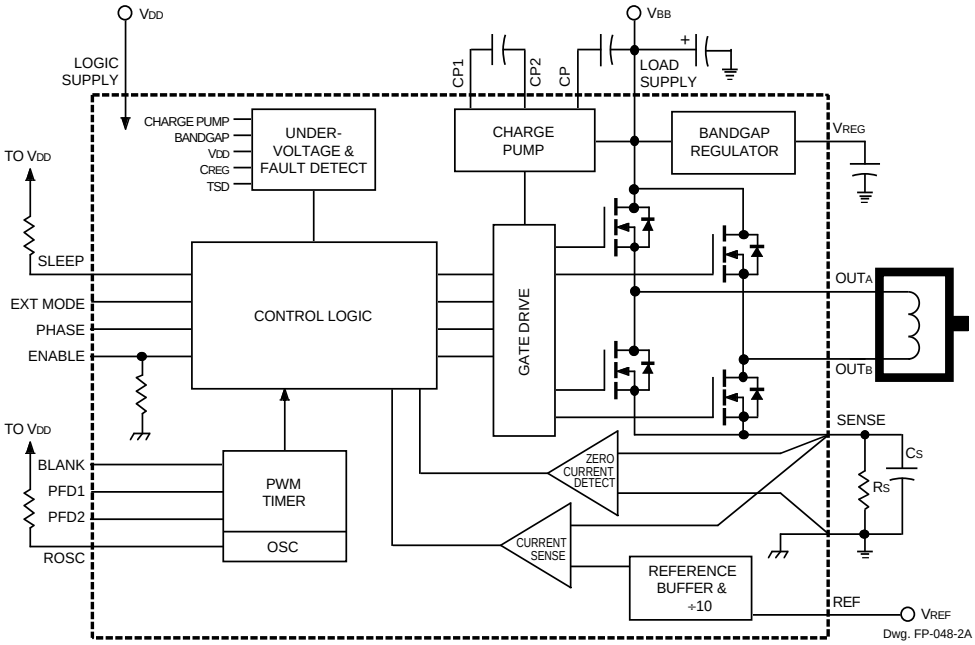
Designed for pulse width modulated (PWM) current control of DC motors, the A3959 is capable of output currents to ±3 A and operating voltages to 50 V. Internal fixed off-time PWM current-control timing circuitry can be adjusted via control inputs to operate in slow, fast, and mixed current-decay modes.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM-control signals. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of supply and charge pump, and crossover-current protection. Special power-up sequencing is not required.

The A3959 provides a choice of three power packages, a 24-pin DIP with batwing tabs (package suffix 'B'), a 24-lead SOIC with four internally-fused pins (package suffix 'LB'), and a thin (<1.2 mm) 28-pin TSSOP with an exposed thermal pad (suffix 'LP'). In all cases, the power pins and tabs are at ground potential and need no electrical isolation. Each package is lead (Pb) free, with 100% matte tin leadframes.

Functional Block Diagram



Selection Guide

Part Number	Package	Packing
A3959SB-T	24-pin DIP with exposed tabs	15 per tube
A3959SLB-T	24-pin SOIC with internally fused pins	31 per tube
A3959SLBTR-T	24-pin SOIC with internally fused pins	1000 per reel
A3959SLP-T	28-pin TSSOP with exposed thermal pad	50 per tube
A3959SLPTR-T	28-pin TSSOP with exposed thermal pad	4000 per reel

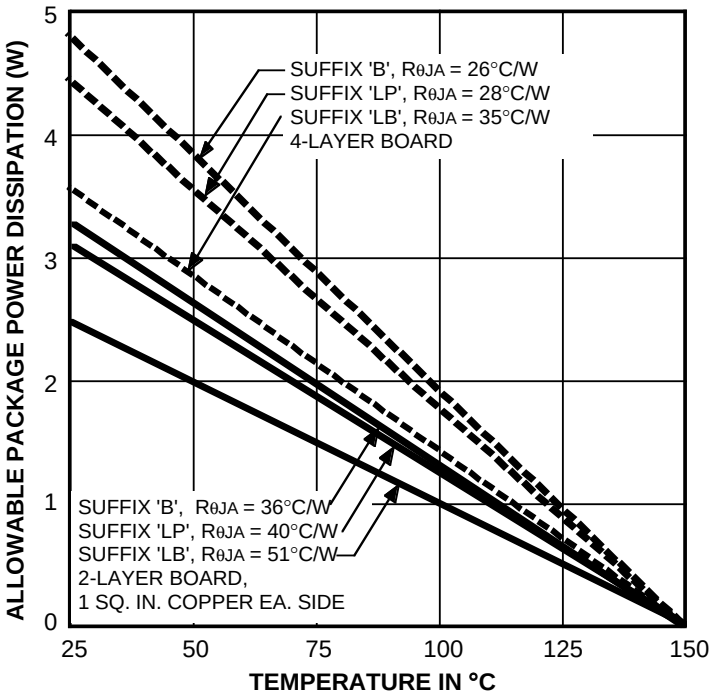
Absolute Maximum Ratings

Characteristic	Symbol	Notes		Rating	Units
Load Supply Voltage	V_{BB}			50	V
Logic Supply Voltage	V_{DD}			7.0	V
Input Voltage	V_{IN}	Continuous		–0.3 to V_{DD} + 0.3	V
		t_w < 30 ns		–1.0 to V_{DD} + 1.0	V
Sense Voltage	V_S	Continuous		0.5	V
		t_w < 3 µs		2.5	V
Reference Voltage	V_{REF}			V_{DD}	V
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	Repetitive	±3.0	A
			Peak, < 3 µs	±6.0	A
Package Power Dissipation	P_D	See Thermal Characteristics		–	–
Operating Ambient Temperature	T_A	Range S		–20 to 85	ºC
Maximum Junction Temperature	T_J(max)	Fault conditions that produce excessive junction temperature will activate the device's thermal shutdown circuitry. These conditions can be tolerated but should be avoided.		150	ºC
Storage Temperature	T_{stg}			–55 to 150	ºC

Thermal Characteristics

Characteristic	Symbol	Test Conditions		Value	Units
Package Power Dissipation	P_D	B package		3.3	W
		LB package		2.5	W
		LP package		3.1	W
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	B Package	1-layer PCB, minimal exposed copper area	54	ºC/W
			2-layer PCB, 1-in^2 2-oz copper exposed area	36	ºC/W
			4-layer PCB, based on JEDEC standard	26	ºC/W
		LB Package	1-layer PCB, minimal exposed copper area	77	ºC/W
			2-layer PCB, 1-in^2 2-oz copper exposed area	51	ºC/W
			4-layer PCB, based on JEDEC standard	35	ºC/W
		LP Package	1-layer PCB, minimal exposed copper area	100	ºC/W
			2-layer PCB, 1-in^2 2-oz copper exposed area	40	ºC/W
			4-layer PCB, based on JEDEC standard	28	ºC/W
Package Thermal Resistance, Junction to Tab	$R_{\theta JT}$	B and LB packages		6	ºC/W
Package Thermal Resistance, Junction to Pad	$R_{\theta JP}$	LP package		2	ºC/W

*Additional thermal information available on Allegro website.



ELECTRICAL CHARACTERISTICS (continued) at T_A = +25°C, V_{BB} = 50 V, V_{DD} = 5.0 V, V_{SENSE} = 0.5 V, f_{PWM} < 50 kHz (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Reference Divider Ratio	–		–	10	–	–
Gm Error (Note 3)	E_{Gm}	$V_{REF} = V_{DD}$	–	–	±4.0	%
		V_{REF} = 0.5 V	–	–	±14	%
Propagation Delay Times	t_{pd}	0.5 E_{in} to 0.9 E_{out}:				
		PWM change to source on	600	750	1200	ns
		PWM change to source off	50	150	350	ns
		PWM change to sink on	600	750	1200	ns
		PWM change to sink off	50	100	150	ns
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold	UVLO	Increasing V_{DD}	3.90	4.2	4.45	V
UVLO Hysteresis	ΔUVLO		0.05	0.10	–	V

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.
3. G_m error = $([V_{REF}/10] – V_{SENSE})/(V_{REF}/10)$ where $V_{SENSE} = I_{TRIP} \bullet R_S$.

FUNCTIONAL DESCRIPTION

V_{REG}. This internally generated voltage is used to operate the sink-side DMOS outputs. The V_{REG} terminal should be decoupled with a 0.22 µF capacitor to ground. V_{REG} is internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Charge Pump. The charge pump is used to generate a gate-supply voltage greater than V_{BB} to drive the source-side DMOS gates. A 0.22 µF ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.22 µF ceramic capacitor should be connected between CP and V_{BB} to act as a reservoir to operate the high-side DMOS devices. The CP voltage is internally monitored and, in the case of a fault condition, the source outputs of the device are disabled.

PHASE Logic. The PHASE input terminal determines if the device is operating in the "forward" or "reverse" state.

PHASE	OUT_A	OUT_B
0	Low	High
1	High	Low

ENABLE Logic. The ENABLE input terminal allows external PWM. ENABLE high turns on the selected sink-source pair. ENABLE low switches off the source driver or the source and sink driver, depending on EXT MODE, and the load current decays. If ENABLE is kept high, the current will rise until it reaches the level set by the internal current-control circuit.

ENABLE	Outputs
0	Chopped
1	On

EXT MODE Logic. When using external PWM current control, the EXT MODE input determines the current path during the chopped cycle. With EXT MODE low, fast decay mode, the opposite pair of selected outputs will be enabled during the off cycle. With EXT MODE high, slow decay mode, both sink drivers are on with ENABLE low.

EXT MODE	Decay
0	Fast
1	Slow

Current Regulation. Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the DMOS H bridge are turned on, the current increases in the motor winding until it reaches a trip value determined by the external sense resistor (R_S) and the applied analog reference voltage (V_{REF}):

$$I_{TRIP} = V_{REF}/10R_S$$

At the trip point, the sense comparator resets the source-enable latch, turning off the source driver. The load inductance then causes the current to recirculate for the fixed off-time period. The current path during recirculation is determined by the configuration of slow/mixed/fast current-decay mode via PFD1 and PFD2.

Oscillator. The PWM timer is based on an internal oscillator set by a resistor connected from the R_{OSC} terminal to V_{DD}. Typical value of 4 MHz is set with a 51 kΩ resistor. The allowable range of the resistor is from 20 kΩ to 100 kΩ.

$$f_{OSC} = 204 \times 10^9/R_{OSC}.$$

If R_{OSC} is not pulled up to V_{DD}, it must be shorted to ground.

Fixed Off Time. The A3959 is set for a fixed off time of 96 cycles of the internal oscillator, typically 24 µs with a 4 MHz oscillator.

FUNCTIONAL DESCRIPTION (continued)

Internal Current-Control Mode. Inputs PFD1 and PFD2 determine the current-decay method after an overcurrent event is detected at the SENSE input. In slow-decay mode, both sink drivers are turned on for the fixed off-time period. Mixed-decay mode starts out in fast-decay mode for a portion (15% or 48%) of the fixed off time, and then is followed by slow decay for the remainder of the period.

PFD2	PFD1	% t_{off}	Decay
0	0	0	Slow
0	1	15	Mixed
1	0	48	Mixed
1	1	100	Fast

PWM Blank Timer. When a source driver turns on, a current spike occurs due to the reverse-recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source-enable latch, the sense comparator is blanked. The blank timer runs after the off-time counter to provide the blanking function. The blank timer is reset when ENABLE is chopped or PHASE is changed. For external PWM control, a PHASE change or ENABLE on will trigger the blanking function. The duration is determined by the BLANK input and the oscilator.

BLANK	t_{blank}
0	$6/f_{osc}$
1	$12/f_{osc}$

Synchronous Rectification. When a PWM off cycle is triggered, either by an ENABLE chop command or internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. The A3959 synchronous rectification feature will turn on the appropriate pair of DMOS outputs during the current decay and effectively short out the body diodes with the low $r_{DS(on)}$ driver. This will reduce power dissipation significantly and can eliminate the need for external Schottky diodes.

Synchronous rectification will prevent reversal of load current by turning off all outputs when a zero-current level is detected.

Shutdown. In the event of a fault (excessive junction temperature, or low voltage on CP or V_{REG}) the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD}, the UVLO circuit disables the drivers.

Braking. The braking function is implemented by driving the device in slow-decay mode via EXTMODE and applying an enable chop command. Because it is possible to drive current in either direction through the DMOS drivers, this configuration effectively shorts out the motor-generated BEMF as long as the ENABLE chop mode is asserted. It is important to note that the internal PWM current-control circuit will not limit the current when braking, because the current does not flow through the sense resistor. The maximum brake current can be approximated by V_{BEMF}/R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worst-case braking situations of high speed and high inertial loads.

SLEEP Logic. The SLEEP input terminal is used to minimize power consumption when when not in use. This disables much of the internal circuitry including the regulator and charge pump. Logic low will put the device into sleep mode, logic high will allow normal operation.

Note: If the sleep mode is not used, connect a 5 kΩ pull-up resistor between the SLEEP terminal and V_{DD}.

FUNCTIONAL DESCRIPTION (continued)

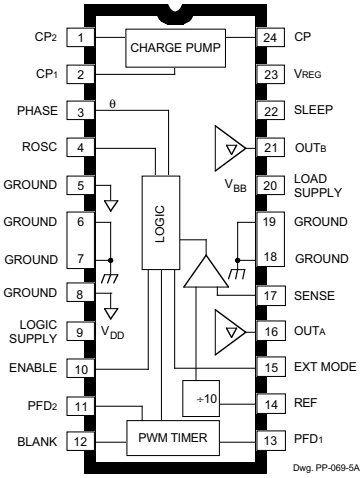
Current Sensing. To minimize inaccuracies in sensing the I_{TRIP} current level, which may be caused by ground trace IR drops, the sense resistor should have an independent ground return to the ground terminal of the device. For low-value sense resistors the IR drops in the PCB sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

The maximum value of R_S is given as $R_S = 0.5/I_{TRIP}$.

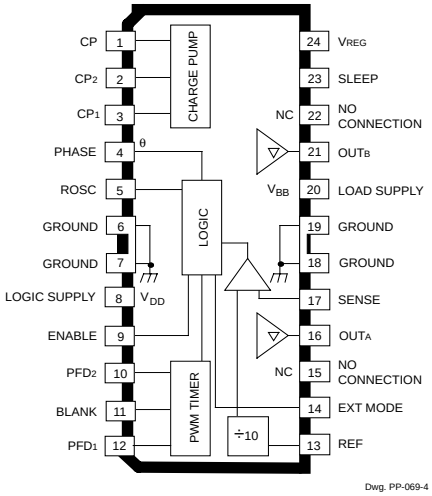
Thermal Protection. Circuitry turns off all drivers when the junction temperature reaches 165°C typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Layout. A star ground system located close to the driver is recommended. The printed wiring board should use a heavy ground plane. For optimum electrical and thermal performance, the driver should be soldered directly onto the board. The ground side of R_S should have an individual path to the ground terminals of the device. This path should be as short as is possible physically and should not have any other components connected to it. It is recommended that a 0.1 µF capacitor be placed between SENSE and ground as close to the device as possible; the load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (> 47 µF is recommended) placed as close to the device as is possible. On the 28-lead TSSOP package, the copper ground plane located under the exposed thermal pad is typically used as a star ground.

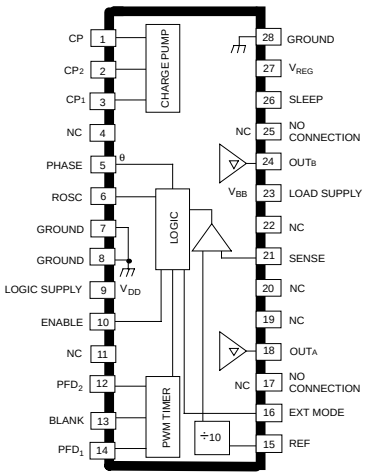
Package B (DIP)



Package LB (SOIC)



Package LP (TSSOP)

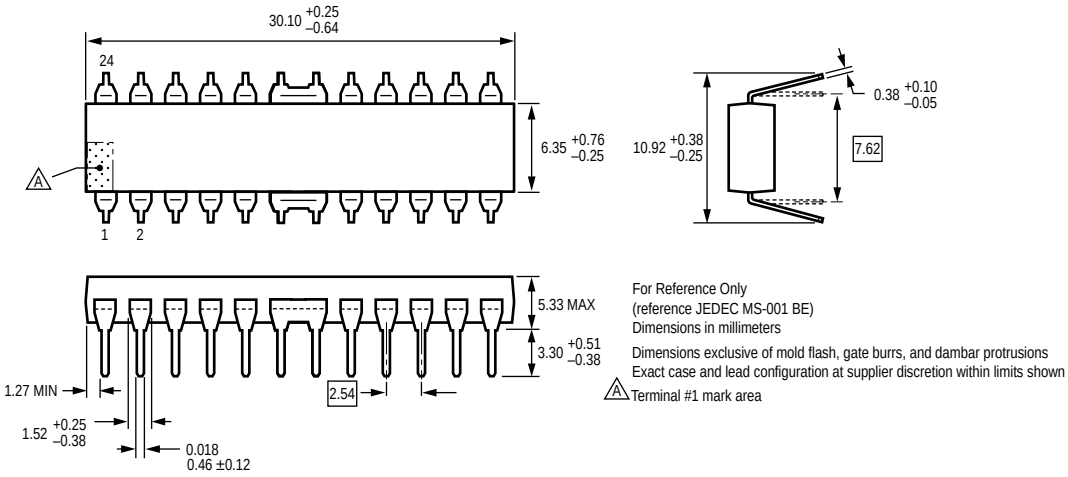


Terminal List

Terminal Name	Terminal Description	B (DIP)	LB (SOIC)	LP (TSSOP)
CP	Reservoir capacitor (typically 0.22 µF)	24	1	1
CP1 & CP2	The charge pump capacitor (typically 0.22 µF)	1 & 2	2 & 3	2 & 3
NC	No (internal) connection	—	—	4
PHASE	Logic input for direction control	3	4	5
ROSC	Oscillator resistor	4	5	6
GROUND	Grounds	5, 6, 7, 8*	6, 7	7, 8*
LOGIC SUPPLY	VDD, the low voltage (typically 5 V) supply	9	8	9
ENABLE	Logic input for enable control	10	9	10
NC	No (internal) connection	–	–	11
PFD2	Logic-level input for fast decay	11	10	12
BLANK	Logic-level input for blanking control	12	11	13
PFD1	Logic-level input for fast decay	13	12	14
REF	VREF, the load current reference input voltage	14	13	15
EXT MODE	Logic input for PWM mode control	15	14	16
NO CONNECT	No (Internal) connection	—	15	17
OUTA	One of two DMOS bridge outputs to the motor	16	16	18
NC	No (internal) connection	–	–	19, 20
SENSE	Sense resistor	17	17	21
NC	No (internal) connection	–	–	22
GROUND	Grounds	18, 19*	18, 19	—
LOAD SUPPLY	VBB, the high-current, 9.5 V to 50 V, motor supply	20	20	23
OUTB	One of two DMOS bridge outputs to the motor	21	21	24
NO CONNECT	No (Internal) connection	—	22	25
SLEEP	Logic-level Input for sleep operation	22	23	26
VREG	Regulator decoupling capacitor (typically 0.22 µF)	23	24	27
GROUND	Ground	—	—	28*

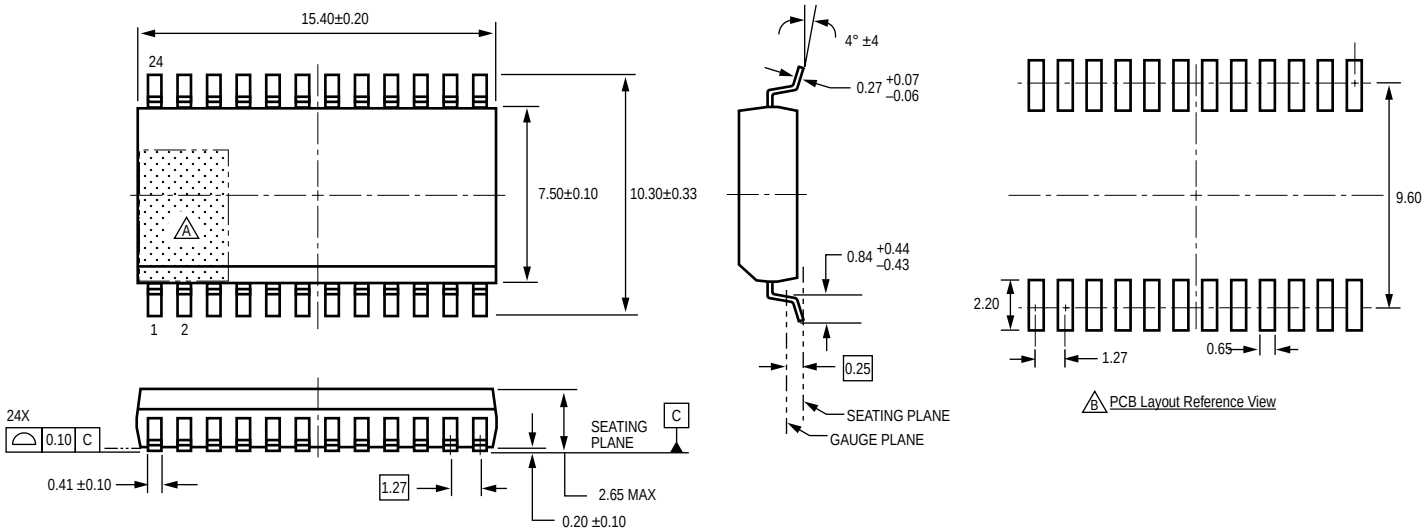
* For the B (DIP) package only, there is an indeterminate resistance between the substrate grounds (pins 6, 7, 18, and 19) and the grounds at pins 5 and 8. Pins 5 and 8, and 6, 7, 18, or 19 must be connected together externally. For the LP (TSSOP) package, the grounds at terminals 7, 8, and 28 should be connected together at the exposed pad beneath the device.

B package 24-pin DIP



For Reference Only
(reference JEDEC MS-001 BE)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

LB package 24-pin SOICW

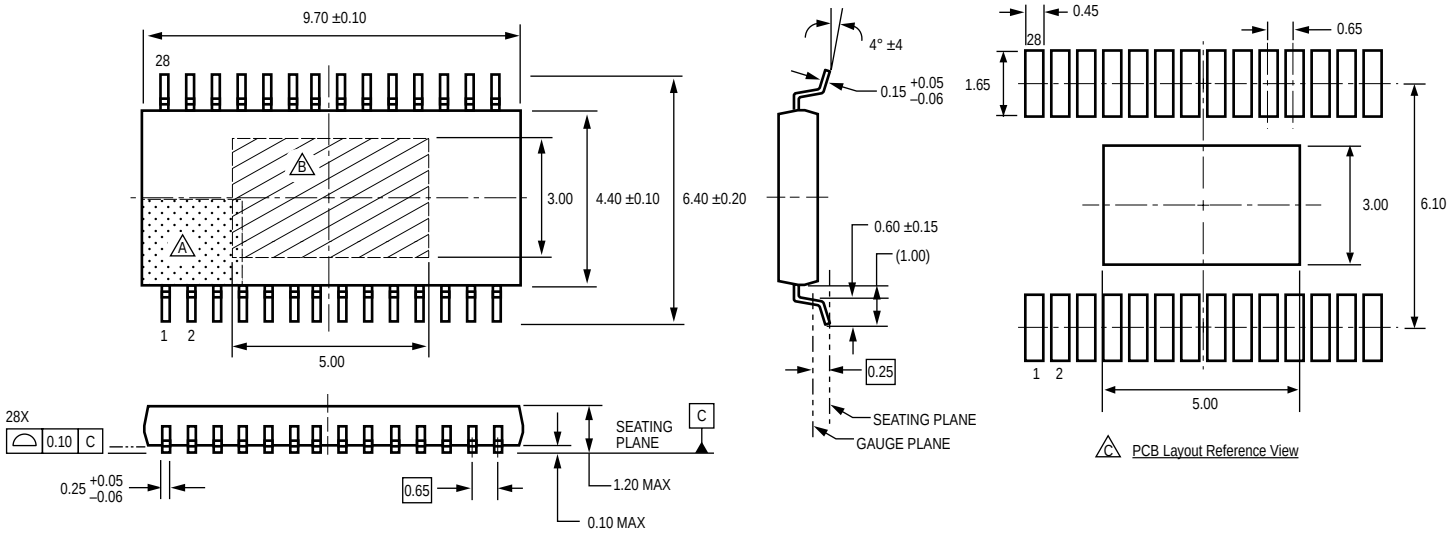


For reference only
Pins 6 and 7, and 18 and 19 internally fused
Dimensions in millimeters
(Reference JEDEC MS-013 AD)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

LP package 28-pin TSSOP



For reference only
(reference JEDEC MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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